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EXAMINER	
HUBER, ROBERT T	

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2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,346	NAMBA ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 9, 2008 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1 – 11 and 13 – 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, claims 1 and 15 recite "*an electron concentration of said first diamond semiconductor exhibits a negative correlation with temperature, in a temperature range having a width of 100°C or more and included within a temperature region from 0°C to 300°C*", which is a property of the device, however the Applicants have not provided a substantial disclosure to support such a claim. Although the

Applicants have recited in the specification numerous times, as well as in the remarks filed on December 9, 2008, that the device has a single layer with the claimed properties, the specification does not indicate how or why such properties exist. The Applicants claim the properties of a "new" material without adequately describing the new material and accounting for such properties. Hence, the claimed invention does not enable one of ordinary skill in the art to make or use such an invention. Claims 2 – 11 and 13 depend on claim 1, and claim 16 depends on claim 15.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 6, 8, 11, and 13 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Imai et al. (US 5,001,452).

a. Regarding claim 1, **Imai discloses a diamond n-type semiconductor** (e.g. Example 1, being in col. 4, line 66) **comprising a first diamond semiconductor which has n-type conduction** (col. 4, line 68 – col. 5, line discloses forming an n-type diamond semiconductor layer, doped with sulfur, on a diamond substrate) **and in which a distortion or defect is artificially formed** (as disclosed in Imai, the n-type layer is doped with dopants (S), and therefore a distortion may be formed in the lattice due to the impurity. Furthermore, the

patentability of a product does not depend on the method of production. See MPEP 2113).

wherein said first diamond semiconductor has an n-type dopant concentration adjusted by vapor-phase growth (col. 5, line 3 discloses forming the n-type dopant concentration layer by CVD, which is a vapor phase deposition. Furthermore, the patentability of a product does not depend on the method of production. See MPEP 2113.) **such that an electron concentration of said first diamond semiconductor exhibits a negative correlation with temperature, in a temperature range having a width of 100°C or more and included within a temperature region from 0°C to 300°C** (see below).

b. Claim 2, **Imai discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor has a Hall coefficient exhibiting a positive correlation with temperature, in the temperature range**

c. Claim 3, **Imai discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein the temperature range included within the temperature region from 0°C to 300°C has a width of over 200°C or more** (see below)

d. Claim 4, **Imai discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor has a resistivity of 500 Ωcm or less at a temperature within the temperature region from 0°C to 300°C** (see below)

e. Claim 5, **Imai discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein the electron concentration of said first diamond semiconductor is always 10^{16} cm^{-3} or more in the temperature region from 0°C to 300°C** (see below)**.**

Regarding claims 1 – 5, the device of Example 1 of Imai contains an n-type diamond semiconductor layer containing a Sulfur dopant concentration, as disclosed in col. 2, lines 30 – 32 and Table 1, which resides on a diamond substrate, as disclosed in col. 5, lines 1 - 2. Since the device of Imai meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claims 1 - 5, are presumed inherent to the device of Imai. See MPEP 2112.01.

f. Regarding claim 6, **Imai discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor contains more than 5 x 10^{19} cm^{-3} in total of at least one kind of donor element** (col. 2, lines 30 – 32 and Table 1 disclose a dopant

concentration to be between 1 x 10^{12} cm^{-3} and 1 x 10^{21} cm^{-3}, and therefore anticipates the claimed value).

g. Regarding claim 8, **Imai discloses a diamond n-type semiconductor according to claim 6, as cited above, wherein said first diamond semiconductor contains at least S (sulfur) as the donor element** (e.g. as disclosed in col. 4, line 68).

h. Regarding claim 11, **Imai discloses a diamond n-type semiconductor according to claim 1, wherein said first diamond semiconductor is monocrystal diamond** (e.g. col. 2, line 28 discloses the formation of the first diamond semiconductor by "single-crystal" growth).

i. Regarding claim 13, **Imai discloses a semiconductor device at least partly employing a diamond n-type semiconductor according to claim 1** (as disclosed in col. 4, lines 38 - 44)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Hasegawa et al. (US 2002/0127405 A1, prior art of record). **Imai discloses the diamond semiconductor according to claim 6, as cited above, but is silent with respect to explicitly disclosing said first diamond semiconductor contains at least P (phosphorus) as the donor element. However, Imai does acknowledge that phosphorus may be used as a dopant in semiconductors** (col. 2, lines 20 - 21).

Hasegawa discloses that both phosphorus and sulfur can be used as n-type dopants in diamond semiconductors (e.g. ¶ [0032] discloses the use of sulfur, and ¶ [0037] discloses that phosphorus may also be used).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Imai such that phosphorus was uses as the dopant in the n-type diamond semiconductor layer since Imai discloses that sulfur is used as the n-type dopant, and Hasegawa discloses that both sulfur and phosphorus

may be used as the n-type dopant in the diamond semiconductor. One would have been motivated to use phosphorus instead of sulfur in order to adjust the band-gap and electrical properties of the semiconductor to optimize the semiconductor properties, such as conductivity, for a desired circuit, as discussed by Hasegawa (¶ [0037]).

9. Claims 9, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Yoshida (US 6,340,393 B1, prior art of record).

a. Regarding claim 9, **Imai discloses a diamond n-type semiconductor according to claim 1, as cited above, however Imai is silent with respect to said first diamond semiconductor containing an impurity element other than the donor element together with the donor element.**

Yoshida discloses a combining a second impurity element together with the donor element in a diamond semiconductor (col. 2, lines 51 – 52, col. 5, lines 59 – 61, and col. 5, lines 65 - 67).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Imai to include a second impurity element along with the donor element, since it was known that one may combine second impurity elements into doped diamond semiconductor materials, as taught by Yoshida, because it would allow a stabilization of the semiconductor layer with a large dopant density (as discussed in Yoshida, col. 2, lines 51 - 53).

b. Regarding claim 14, **Imai discloses the diamond n-type semiconductor according to claim 1, as cited above, but is silent with respect to the device being used in at least an electron emitting part of an electron emitting device.**

Yoshida discloses that diamond semiconductor devices can be used as an electron emitter (col. 5, lines 18 – 19).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use the diamond semiconductor of Imai as an electron emitter since Yoshida discloses that such semiconductor devices can be used as electron emitters. One would be motivated to use the devices in such a manner since a low resistivity exists in such devices, creating an efficient electron emitter.

c. Regarding claim 15, **Imai discloses a method of manufacturing a diamond n-type semiconductor** (e.g. Example 1, being in col. 4, line 66), **said method comprising the steps of:**

preparing a diamond substrate (substrate disclosed in col. 5, line 1); **and**

epitaxially growing a diamond semiconductor on said diamond substrate by vapor phase growth (col. 4, line 68 – col. 5, line 3 discloses forming the diamond semiconductor by CVD (chemical vapor deposition) and col. 2, lines 25 – 26 disclose forming the diamond semiconductor by vapor phase growth. Col. 5, line 8 discloses the diamond semiconductor to be epitaxial),

whereby said diamond semiconductor has n-type conduction (e.g. as disclosed in col. 5, lines 7 - 10) **and has a distortion or defect which is artificially formed therein** (as disclosed in Imai, the n-type layer is doped with dopants (S), and therefore a distortion may be formed in the lattice due to the impurity),

wherein said diamond semiconductor has an n-type dopant concentration adjusted by said vapor-phase growth (col. 4, line 68 – col. 5, line 3 discloses forming the diamond semiconductor by CVD (chemical vapor deposition) and col. 2, lines 25 – 26 disclose forming the diamond semiconductor by vapor phase growth. Table 1 discloses adjusting the n-type dopant concentration). **Imai is silent with respect to disclosing artificially introducing an impurity element other than a donor element to said diamond substrate while growing the diamond semiconductor.**

Yoshida discloses artificially introducing an impurity element other than a donor element to a diamond substrate while growing the diamond semiconductor (e.g. col. 2, lines 51 – 52, col. 5, lines 59 – 61, and col. 5, lines 65 - 67).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the method of Imai such that an impurity element other than the donor (dopant) element is introduced to the diamond substrate while growing the diamond semiconductor since Yoshida discloses that the addition of impurities while growing diamond semiconductors on diamond

substrates can be advantageous. One would have been motivated to add the impurity to the doped diamond semiconductor because it would aid in the stabilization of the diamond semiconductor layer with a large dopant density (as discussed in Yoshida, col. 2, lines 51 - 53).

Regarding the claimed limitation of the electron concentration of said diamond semiconductor exhibiting a negative correlation with temperature, in a temperature range having a width of 100°C or more and which included within a temperature region from 0°C to 300°C, the method of Example 1 of Imai (comprising forming an n-type diamond semiconductor layer containing a concentration of a Sulfur dopant, which resides on a diamond substrate), in view of the method of Yoshida (introducing an impurity element to the to the diamond substrate while growing a doped diamond semiconductor layer), is an obvious teaching over the method of claim 15. Since the method of Imai in view of Yoshida results in the structural limitations of the claimed method invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration, are presumed inherent to the device of Imai in view of Yoshida. See MPEP 2112.01).

10. Claims 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Yoshida as applied to claim 9 above, and further in view of Hasegawa.

a. Regarding claim 10, **Imai in view of Yoshida disclose a diamond n-type semiconductor according to claim 9, as cited above, however they are silent with respect to explicitly disclosing said first diamond semiconductor containing at least 1 x 10^{17} cm^{-3} of Si as the impurity element.**

Hasegawa discloses that a concentration of 1x 10^{16} to 1x10^{21} cm^{-3} of silicon can be used as an impurity element when doping semiconductor diamond (paragraphs [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Imai in view of Yoshida, such that the other impurity element is silicon with a concentration of 1x 10^{16} to 1x10^{21} cm^{-3} since Hasegawa discloses that silicon can be used in such concentrations to dope semiconductor diamond with a p-type material, and Yoshida discloses that a combination of n-type and p-type materials may be doped into a diamond semiconductor in order to stabilize the material when high n-type densities are used (col. 2, lines 50 - 52 of Yoshida). One would be motivated to use silicon as an impurity element since silicon was a commonly used element in the semiconductor industry and is readily available with well-known properties, and one skilled in the art may adjust the band-gap and electrical properties of the semiconductor to using Si to optimize the semiconductor properties, such as conductivity, for a desired circuit, as discussed by Hasegawa (¶ [0037]).

b. Regarding claim 16, **Imai in view of Yoshida disclose a method of forming a diamond n-type semiconductor according to claim 15, as cited above, however they are silent with respect to explicitly disclosing that Si is artificially introduced as the impurity element to said diamond semiconductor substrate.**

Hasegawa discloses that silicon can be used as an impurity element when doping semiconductor diamond (paragraphs [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the method of Imai in view of Yoshida, such that the other impurity element is silicon since Hasegawa discloses that silicon can be used in such concentrations to dope semiconductor diamond with a p-type material, and Yoshida discloses that a combination of n-type and p-type materials may be doped into a diamond semiconductor in order to stabilize the material when high n-type densities are used (col. 2, lines 50 - 52 of Yoshida). One would be motivated to use silicon as an impurity element since silicon was a commonly used element in the semiconductor industry and is readily available with well-known properties, and one skilled in the art may adjust the band-gap and electrical properties of the semiconductor to using Si to optimize the semiconductor properties, such as conductivity, for a desired circuit, as discussed by Hasegawa (¶ [0037]).

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Shiomi et al. (US 5,252,840). **Imai discloses a diamond n-type semiconductor according to claim 1, but is silent with respect to disclosing the device further comprises a second diamond semiconductor provided adjacent to said first diamond semiconductor and turned out to be n-type, wherein said second diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature and a Hall coefficient not exhibiting a positive correlation with temperature, in the temperature range.**

Shiomi discloses that a second diamond semiconductor may be provided adjacent to a first diamond semiconductor (e.g. figure 1(b), second diamond semiconductor 3, disclosed in col. 9, lines 46 – 48, adjacent to first diamond semiconductor 2, disclosed in col. 8, lines 21 - 22),

wherein said second diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature and a Hall coefficient not exhibiting a positive correlation with temperature, in the temperature range (col. 5, lines 16 – 24 disclose the structural characteristics of the device and layers. Since the device of Shiomi meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claim 12, are presumed inherent to the device of Shiomi. See MPEP 2112.01).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Imai such that a second diamond semiconductor layer was adjacent to the first diamond semiconductor layer, with the claimed properties, since Shiomi discloses that one may form such structures to achieve desired conduction properties of the device (col. 9, lines 61 – 68). One would have been motivated to form a second diamond semiconductor layer adjacent to the first diamond semiconductor layer in order to allow charge carrier diffusion from the first layer into the second layer, thereby altering the conduction properties of the device, as disclosed by Shiomi (col. 5, line 16 – 21).

Although Shiomi is silent with respect to the second semiconductor being n-type, Shiomi discloses the first and second diamond semiconductor layers to be p-type doped diamond semiconductor (col. 8, line 22 and col. 9, lines 48 - 49), **and it is well-known in the art that one may interchange p-type and n-type doping to achieve a desired charge carrier concentration of either holes or electrons** (e.g. as discussed in Shiomi, col. 1, lines 51 – 55, and Imai, col. 1, lines 16 - 24). **One would have been motivated to substitute n-type doping for p-type doping in the first and second layers of Shiomi in order to create an n-type device, which would allow one to form complimentary circuits well-known in the semiconductor art (e.g. pn junctions).**

Response to Arguments

12. Applicant's arguments with respect to claims 1 and 15 have been considered but are moot in view of the new ground(s) of rejection. In the Applicants response filed on December 9, 2008 the Applicant argues that the prior art does not disclose or anticipate that the *electron concentration of the semiconductor is negatively correlated with temperature*. Although the Applicant claims a property of the semiconductor structure such as "*an electron concentration negatively correlated with temperature in a temperature range*", the Applicant has not claimed a structure that exhibits such a property. Currently, the device of Imai and the method of Imai in view of Yoshida discloses the claimed structure and method, respectively, and it has been held that when the prior art anticipates or renders obvious the claimed invention, then the properties of the invention may be considered to be inherent to the claimed invention. See MPEP 2112.01: "*Where the claimed and prior art products are identical or substantially identical in structure or composition, or produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established*."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
February 24, 2009